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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,825	12/26/2000	Lance W. Dover	42390P8645	6298

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EXAMINER

NAMAZI, MEHDI

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 03/10/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/748,825

Applicant(s)

DOVER ET AL.

Examiner

Mehdi Namazi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7, 8, and 9</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

This office action is in response to amendment filed December 16, 2003.

Claims

1. Claims 1, 9, 15, 20, and 22 have been amended.

Response to Arguments

2. Applicant's arguments filed December 16, 2003 have been fully considered but they are not persuasive.

In response to applicant's argument on page 15 with regard to claim1 state that:
"The flash memory internal Write state Machine (WSM) automatically verifies data written to the memory. Program verify operations initiated by the ATE are redundant with flash memory internal program verify operations. You can save time by not performing program verify operations with ATE."

Examiner is disagree with applicant's suggestion because "Program verify operations initiated by the ATE are redundant with flash memory internal program verify operations".

In response to applicant's argument on pages 15 and 16 that Olive do not teach the claimed invention. Examiner refers to (column. 2, lines 9-31), where it states that:

"The control circuitry includes an internal state machine, and test circuitry. The test circuitry has disabling circuitry that disables the internal state during a test mode activation phase.....applying circuitry that applies

test signals to the control lines to program the cell matrix during a test performance phase....."

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-25 are provisionally rejected under the judicially created doctrine of obviousness -type double patenting as being unpatentable over claims 1-25 of copending Application No. 09/752,594. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for programming a memory, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing internal

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Program verification, and exiting the special programming mode of the memory, and other limitations or steps such as those directed to enabling internal program verification with the consequent loss of their function, would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made, anticipation being the epitome of obviousness. See particularly claims 1, 4, 13, and 14, for example. Note also that the commonly assigned patent also claims subsequently enabling internal program verification, as well as having a host processor verify external to the memory the programming of the plurality of data words into the memory. The commonly assigned patent also claims disabling entry into the special program mode of the memory, as well as using only a single programming pulse for each bit of each word of the plurality of words, and sending a data word to the memory for reprogramming. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

9. Claims 1-25 are also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/749,133. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for performing programming operations in a memory as in the present invention, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing

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internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to hashing words and comparing hash values, with the consequent loss of their function, would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made. See particularly claims 1, 14 and 17, for example. The commonly assigned patent also claims enabling internal program verification, as well as programming a plurality of words, and using a host processor as a "verification processor" to verify the programming during a special programming mode. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-12, and 15-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel (Simplify Manufacturing by Using Automatic-Test-Equipment for On-Board Programming (AP-629, AP-678), and further in view of Olivo et al. (Olive) (U.S. Patent No. 5,600,600).

As per claim 1, 10, 15, and 22, Intel teaches a method for programming a memory including enabling a "special" or test programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification, was known in the art at the time the claimed invention was made. (Intel, page 9, each taken separately. As one of ordinary skill in the art would readily appreciate, a plurality of words may be programmed into the memory during a "special" or test mode, and the "special" or test-programming mode exited after the tests are performed.

Intel also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (Intel (AP-629), pages 9-10, and Figure 4), Intel further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (Intel (AP-629), page 9, column 2, e.g.).

Intel (AP-678) similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2).

As per claims 1, 15, and 22, Intel teaches the claimed invention, specifically discuss saving time by not performing program verify operations with the external ATE. Intel does not teach disabling internal Program verification operations during the

"special" programming mode so that a plurality of words is programmed in the "special" or test mode without the memory performing internal program verification.

Olivo discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (column 1, lines 26-62; column 2, lines 9-31; and column 4, lines 7-12 32-36). Olivo teaches that overall testing speed may be improved, and that various testing values or parameters may be selected at will so that the memory test can be made fully independent of the control unit and the internal state machine (column 5, lines 1-10, as well as column 1, lines 40-62, e.g.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to disable program verification operations by an internal state machine during a "special" programming mode, as taught by Olivo, in the flash memory of Intel, so that a plurality of words may be programmed without the memory performing internal program verification, because the Intel teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one should consider modifying the method or program flow to perform only necessary operations, and Olivo teaches that an improved testing speed and greater flexibility in the testing process may be obtained by disabling or not performing internal program verification operations. The

improvement in testing speed and ability to change the testing process independent of the control unit and internal state machine as taught by Olivo provides ample motivation and suggestion to disable internal program verification operations in a memory such as in the Intel, so as to avoid redundant program verify operations while providing an improved test speed and increased flexibility in the testing process.

As per claims 2, Intel teaches having a host processor verify external to the memory the programming of the plurality of data word into the memory (Intel AP-629, fig. 2).

As per claims 3, 17, and 24, Intel teaches that the memory is a nonvolatile memory (Intel AP-629), fig. 3, flash memory).

As per claims 4, and 6, Intel teaches, the special programming mode is entered by the host sending a command to the memory for entering the special programming mode (Intel AP-629, page 9, col. 2).

As per claim 5, Intel teaches the special programming mode is exited by the host sending a command to the memory for exiting the special programming mode (AP-629, page 10, col. 1, verify that the desired bits are sufficiently programmed).

As per claim 7, Intel teaches the host processor sends the plurality of words to the memory for programming into the memory (AP-629, page 10, col. 2, lines 1-2).

As per claim 8, Intel teaches disabling further entry into the special program mode of the memory by sending a disable special programming mode command from the host processor to the memory (AP-629, col. 2, lines 3-8, disabling automatically verifying data written to the memory).

As per claim 9, Intel teaches programming a plurality of words into the memory further comprises using only a single programming pulse for programming one or more memory cells corresponding to the plurality of words (it is inherent in any memory to use a certain bit or word per pulse, where each bit is located in a cell).

As per claims 11, and 20, Intel teaches the special algorithm determines width and repetition of a programming pulse to be used during the special programming mode (it is common in memory to have a change of pulse length depended on program or length of data).

As per claim 12, Intel teaches having the host processor verify external to the memory the programming of the plurality of data words into the memory comprises having the host processor read the plurality of words programmed into the memory and compare with a plurality of respective data words stored by the host processor in a second memory (Intel A-629, fig. 2 shows the second memory (main memory or cache could be used, and Intel AP-678, page 7, cols. 1, and 2).

As per claims 16, and 23, Intel teaches, a host processor (Intel, AP-629, fig. 2) comprising: circuitry to enable or disable the special programming mode circuitry of the memory (Intel, AP-678, fig. 1, page 7); circuitry to send to the memory a plurality of data words to be programmed into the memory without the memory performing internal program verification if the special programming mode circuitry is enabled (Intel, AP-678, fig. 2); circuitry to verify external do the memory programming of the plurality of data words into the memory if the special programming mode circuitry is enabled (Intel, AP-678, fig. 2).

As per claim 18, Intel teaches the circuitry to enable or disable special programming mode circuitry comprises circuitry for sending special commands to the memory (Intel, AP-678, page. 7, col. 1, lines 5-9).

As per claims 19, and 25, Intel teaches circuitry to disable further entry into the special programming mode of the memory is disable special programming mode command is sent from the host processor to the memory (Intel, AP-678, fig. 2, and page 7, col. 1, lines 5-9).

As per claim 21, Intel teaches the circuitry to verify external to the memory comprises: a second memory coupled to the host processor storing the plurality of data words (Intel, AP-678, fig. 2, "data queue registers" works as second memory); circuitry for comparing the plurality of data words stored in the second memory with a plurality of data words read from the memory by the host processor (Intel, AP-678, fig. 2, "data comparator").

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 703-306-2758. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi,
Examiner
Art Unit 2188

March 7, 2004

Mano Padmanabhan
3/8/04

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